X-4

A MONOLITHIC X-BAND FOUR-BIT PHASE SHIFTER

Y. Ayasli, A. Platzker*, J. L. Vorhaus, and L. D. Reynolds
Raytheon Company
Research Division
Lexington, Massachusetts 02173
* Missile Systems Division
Bedford, Massachusetts 01730

Abstract

X-band GaAs MMIC passive phase shifters have been developed using FET switches. A four-bit digital phase shifter with 5.1 ± 0.6 dB insertion loss has been realized on a single 6.4 × 7.9 × 0.1 mm chip.

Introduction

The use of FETs as microwave switches has been reported earlier [1]-[4]. In this paper we will describe the use of such FET switches in two different types of GaAs monolithic passive phase shifter bits. We will also describe the fabrication and performance of a single-chip MMIC X-band four-bit passive phase shifter formed by cascading these switch FET circuits. The basic switch element, a single pole-single throw circuit in shunt mode of operation is shown in Fig. 1a. The FET switch is a three-terminal device with the gate voltage V_G controlling the switch states. In a typical switch mode, the high impedance state (switch closed) corresponds to a negative gate bias larger in magnitude than the pinchoff voltage ($|V_g|>|Vp|$), and the low impedance state (switch open) corresponds to zero gate bias. These two linear operation regions of the FET are shown schematically in Fig. 1b. Note that in either state virtually no dc bias power is required. Therefore the switches can practically be classified as passive as far as the overall power consumption is concerned.

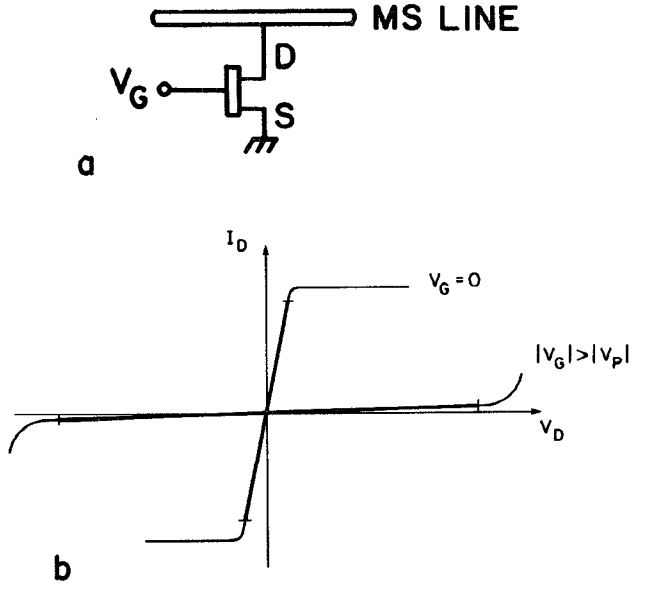


Fig. 1 (a) Basic GaAs switch in shunt mode of operation; (b) Switch FET linear operating regions.

Although the FET itself is a three-terminal device, the switch is bidirectional. The equivalent circuit for the two states of the switch can be represented as shown in Fig. 2. For a typical 1000 μm switch FET,

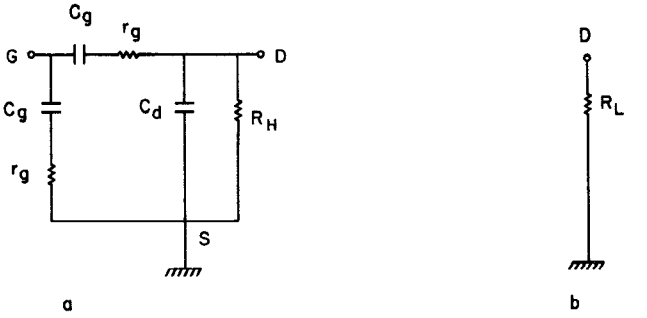


Fig. 2 Approximate equivalent circuit used in the designs for a switch FET. (a) High resistance state; (b) Low resistance state.

the numerical values for the equivalent circuit parameters are shown in Table 1. These values are dependent on the channel geometry, channel doping, and pinchoff voltage of the device.

Note that, unlike the PIN diode, the total capacitor shunting the high impedance R_H represents a reactance of the order of 50 ohms at X-band frequencies. Therefore, to realize the switching action, this capacitance must be either resonated or its effect must be included in the design of the impedance-matching sections. This represents an important design consideration for FET switches as it directly relates to the frequency bandwidth of operation.

TABLE 1
TYPICAL EQUIVALENT CIRCUIT PARAMETERS FOR 1 mm TOTAL PERIPHERY SWITCH FET

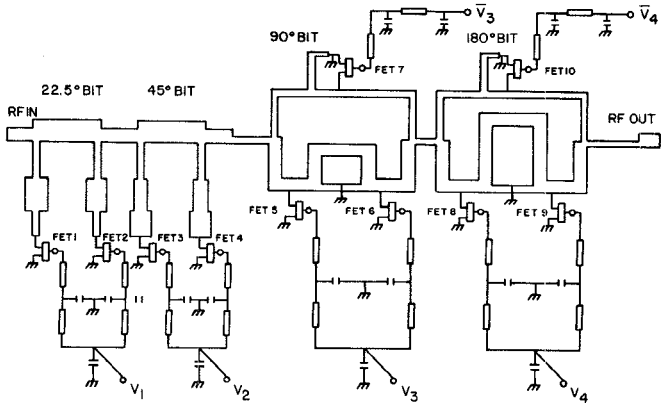
R_L	:	3 ohm
R_H	:	3 Kohm
C_d	:	0.2 pF
r_g	:	1.6 ohm
C_g	:	0.2 pF

Four-Bit Phase-Shifter Circuit

The schematic circuit diagram of the four-bit phase shifter is shown in Fig. 3. The 22.5 and 45 degree bits are designed to provide constant phase shifts over the frequency bandwidth using the loaded line technique. Each loading stub is composed of a suitably designed transforming and matching network which is terminated by a 1200 μm switch FET. The principle of operation of our circuits and of the ones using PIN diodes is the same. Both utilize the fact that the phase of a signal passing through a loaded transmission line is a function of that load. A phase shift is obtained when the load is altered between two states. If the main line is symmetrically loaded, it is possible to obtain, over appreciable bandwidths, phase shifts at approximately constant insertion losses and low input and output VSWR. In order to

0149-645X/82/0000-0486 $00.75 © 1982 IEEE

do so, the loads seen by the main rf line at the two phase states must assume two distinct values. In general, the impedances of the switching elements, whether they are PIN diodes or MESFETs, do not present the proper impedances to the main line and thus require transformation. The transformation is bilinear and its physical realization constitutes the design of the circuits.



FET1 to FET4 : 1200 μm gate periphery
FET5 to FET10 : 800 μm gate periphery
All capacitors : Si_3N_5, 3 pF each
Control Voltages: 0, -7 Volts

Fig. 3 The schematic circuit diagram of the 4-bit phase shifter.

The 90° and 180° bits are designed using the switched-line technique. Switching between lines of different electrical lengths is accomplished by two single-pole double-throw (SPDT) switches similar in principle of operation to the X-band bidirectional switch reported earlier [4]. Note, however, that instead of the conventional four switching elements, only three 800 μm switch FETs are used in these circuits. Equal insertion loss between two phase states is maintained by designing the short and long arms of the phase shifter at different impedance levels.

For all bits, the switching is performed only through the gate control voltages and no other bias is required for the operation of the phase shifter. Thus rf microstrip lines do not carry any dc voltage (in fact they are dc grounded) and therefore there is no need for dc blocking capacitors between individual phase bit circuits.

The four bits are cascaded to form a complete phase shifter on a single 6.4 × 7.9 × 0.1 mm GaAs chip (Fig. 4). Starting in the upper right with the 180° bit, the microwave signal travels counterclockwise through the 45° (upper left), 22.5° (lower left) and 90° (lower right) bits, exiting on the right edge of the chip. The circuit is passive and reciprocal so that the signal can equally well traverse this path in the opposite direction.

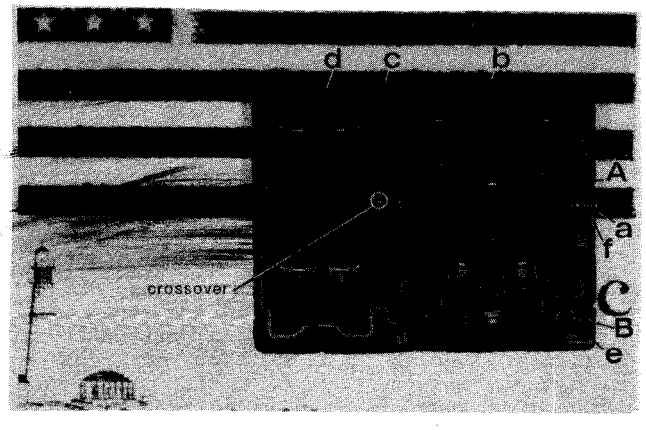


Fig. 4 Four-bit passive phase shifter chip.

TABLE 2

FOUR-BIT PASSIVE PHASE SHIFTER RF AND CONTROL SIGNAL PORTS

A	-	rf input/output
B	-	rf output/input
a	-	180° bit reference arm control signal
b	-	180° bit phase delay arm control signal
c	-	22.5° bit control signal
d	-	45° bit control signal
e	-	90° bit reference arm control signal
f	-	90° bit phase delay arm control signal

The FET devices in each bit have a total gate periphery of 2.4 mm. As shown in the figure and identified in Table 2, there are two control lines for each of the larger bits and one control line for each of the smaller bits. Also seen in the figure is the one crossover necessary in the circuit where the rf line between the 180° and 45° bits crosses the line connecting the control port of the 22.5° bit with the chip edge. All the necessary gate bias circuitry including rf bypass capacitors is provided monolithically on the GaAs chip, with integral beam leads for rf and control lines at the edge of the chip. The four-bit passive phase shifter chip statistics are summarized in Table 3.

TABLE 3

FOUR-BIT PASSIVE PHASE SHIFTER STATISTICS

Chip Size: 6.4 x 7.9 x 0.1 mm
Number of Ports (all have integral beam leads):
rf: 2
Control Signal: 6
Number of FETs: 10
Total Gate Periphery (Gate Length = 1 μm): 9.6 mm
Number of Capacitors (3 pF each): 16
Number of Air Bridges: 77
Number of Via Holes: 26
Total Transmission Line Length: 13.9 cm (5.5 in.)

Circuit Fabrication

Circuits are processed on vapor phase epitaxy layers grown by the $AsCl_3$ system on semi-insulating GaAs substrates. The three-layer structures consist of a high-doped contact layer ($n > 2 \times 10^{18}$ cm^{-3}, $t = 0.2$ μm), an active layer of moderate doping ($n = 9 \times 10^{16}$ cm^{-3}, $t = 0.4$ μm), and an undoped buffer region ($n < 5 \times 10^{13}$ cm^{-3}, $t = 2.0$ μm). Device isolation is achieved with a combination of a shallow mesa etch and a damaging $^{16}O^{+}$ implant.

Ohmic contacts are formed by alloying the standard Ni/AuGe metalization into the surface. The ohmic metal also forms the bottom plates of the thin-film capacitors. The gates, which are recessed, consist of a Ti/Pt/Au (1000/1000/3000 Å) metalization and are nominally 1 μm long.

The capacitor dielectric is a plasma-assisted CVD_o silicon nitride layer with a nominal thickness of 5000 A and dielectric constant of 6.8. The final frontside processing steps define the transmission line structures, capacitor top plates, and air-bridge interconnects. All of these are fabricated out of plated gold about 3 to 4 μm thick. Air-bridges are used to connect from the GaAs surface to the top plates of the MIM capacitors without having to cross the dielectric step and risk shorting of the structure.

After plating, the wafer is mounted upside down on an alumina substrate and is lapped to its final thickness of 100 μm. Via-holes are etched through the wafer to ground points on the frontside. The via-holes are aligned by looking through the slice with infrared optics to see the frontside pattern. Finally, a chip dicing grid is defined in the back by alignment to the via-hole pattern and the region between the grid lines (the chip back) is gold plated to a thickness of 12 to 15 μm. The grid lines are etched through to the frontside, the wafer dismounted and the chips allowed to simply fall apart.

Experimental Performance

Figure 5 shows the insertion loss (not corrected for approximately 1 dB of jig losses) for all 16 states.

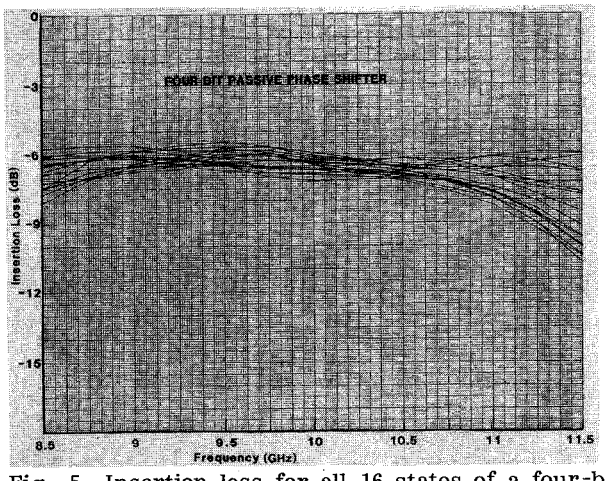


Fig. 5 Insertion loss for all 16 states of a four-bit passive phase shifter (no correction for jig losses has been made).

At 9.5 GHz, the insertion loss is 5.1 ± 0.6 dB. Fig. 6 shows the differential phase shift in the 8.5-10.5 GHz frequency band. Table 4 summarizes the total rms phase error of the four-bit phase shifter and the predicted performance of a typical airborne phased-array antenna system utilizing this monolithic phase shifter. The results indicate that the predicted performance is satisfactory for typical phase array requirements.

Conclusion

An X-band GaAs monolithic phase shifter with 22.5°, 45°, 90°, and 180° phase bits has been made using GaAs switch FETs. By cascading all four bits on the same chip, a digital passive phase shifter with 5.1 ± 0.6 dB insertion loss and 16 distinct phase states between 0° and 360° has been realized. The performance of the phase shifter is satisfactory for typical phased-array applications. Their small sizes, negligible dc power requirements, and subnanosecond switching times make these monolithic phase shifters prime candidates for future frequency-agile airborne phased-array systems.

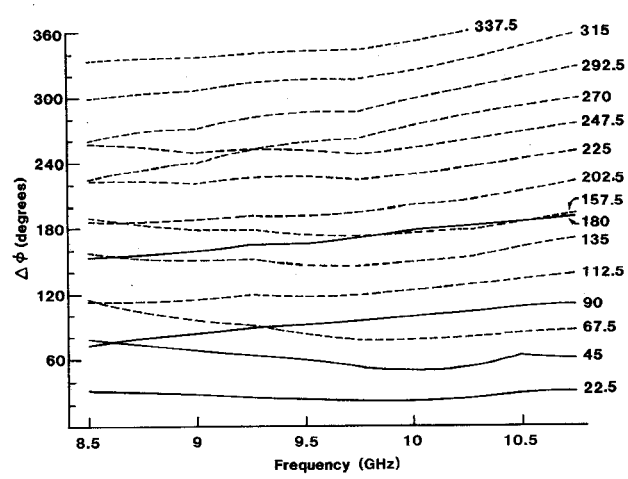


Fig. 6 Phase shift vs. frequency for all 15 non-zero states of a four-bit passive phase shifter.

TABLE 4

ARRAY RANDOM ERROR EFFECTS BASED ON FOUR-BIT PASSIVE MONOLITHIC PHASE SHIFTER DATA

(100 Array Elements are Assumed)

Frequency (GHz)	8.0	8.5	9.0	9.5	10.0	10.5	11.0	11.5	12.0
Total rms Phase Error (σ_T)	39.4°	25.4°	17.3°	11.4°	8.7°	11.1°	14.7°	17.6°	13.1°
Gain Reduction (dB) (G/G_0)	-1.7	-0.8	-0.4	-0.2	-0.1	-0.2	-0.3	-0.4	-0.5
rms Sidelobe Level (dB) (SLL)	-23.3	-27.1	-30.4	-34.0	-36.4	-34.3	-31.8	-33.9	-29.5
Beam Pointing Error (%) $\frac{\Delta\theta}{\theta}_{3\ dB}$	6.9	4.4	3.0	2.0	1.5	1.9	2.6	3.1	3.3

References

1. R. A. Gaspari and H. H. Yee, "Microwave GaAs FET switching," 1978 IEEE International Microwave Symposium Digest, pp. 58-60.

2. W. V. McLevige and V. Sokolov. "Microwave switching with parallel-resonated GaAs FETs," IEEE Electron Device Letter EDL-1, No. 8, Aug. 1980.

3. Y. Ayasli, R. A. Pucel, J. L. Vorhaus, W. Fabian, "A monolithic X-band single-pole, double-throw bidirectional GaAs FET switch," IEEE GaAs Integrated Circuits Symposium, Nov. 4-6, 1980, Las Vegas, Nevada.

4. Y. Ayasli, J. L. Vorhaus, R. A. Pucel, L. D. Reynolds, "Monolithic GaAs distributed FET switch circuits," IEEE GaAs Integrated Circuit Symposium, Oct. 27, 1981, San Diego, California.